REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 5 through 15, 18, and 22 remain in this case. Claims 5 through 12, 18, and 22 are amended. Claims 16, 17, and 19 are canceled in this paper.

Claims 5 through 7 were rejected under §102 as anticipated by the Leary et al. reference[1]. Claims 8 through 19 and 22 were rejected under §103 as unpatentable over the Leary et al. reference.

Claims 16, 17, and 19 are canceled in this paper, obviating the rejection thereof.

Claim 5 is amended to overcome the rejection. Amended claim 5 now further requires the step of operating the target DSP chip according to an application program, during which a count of occurrences of at least one object is accumulated in at least one counter at the target DSP. The claimed method further requires the transferring of the contents of that at least one counter to the host, and processing and interpreting statistics responsive to these contents, at the host. The specification clearly supports this amendment to claim 5,[2] and as such no new matter is presented by this amendment.

Dependent claims 6 and 7 are amended to now depend on claim 5, and to consistently recite their additional limitations relative to amended claim 5, upon which they now depend. Claim 18 is amended to now directly depend upon claim 5, considering the cancellation of claim 17 upon which it previously depended.

The method of amended claim 5 provides important advantages in the analysis and development of application programs for digital signal processors. As discussed in the

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[1] U.S. Patent No. 5,375,228, issued December 20, 1994 to Leary et al.

[2] *See* specification of S.N. 09/845,636 at page 10, line 4 through page 12, line 20; page 13, line 21 through page 14, line 21.

specification,[3] the claimed method enables real-time analysis of a target DSP with as much of the monitoring and analysis offloaded to the host computer; the target device is only required to preserve a minimum amount of data to support the analysis at the host. As a result, the analysis performed at the host closely matches the actual performance of the target DSP in an actual system, permitting the configuration of the target DSP operating system as a result.[4]

Applicants respectfully submit that amended claim 5, and its dependent claims, are novel and patentably distinct over the Leary et al. reference. Nowhere does the Leary et al. reference anywhere disclose the step of accumulating a count of occurrences of an object in a counter at the target DSP, nor the transferring of the contents of this counter to the host for processing and interpreting, as required by amended claim 5.

The Leary et al. reference is directed to an emulation system in which a digital signal analyzer is connected directly to the inputs and outputs of the target DSP device.[5] To the extent that occurrences of an event are accumulated in the Leary et al. system, these occurrences are acquired by the host, emulating, system,[6] which effectively operates in parallel with the target DSP, and "upon the same samples of the analog input and output signals that are being processed by the target system"[7]. According to the Leary et al. reference, therefore, there is no accumulating of any count of occurrences at the target DSP, much less transferring of this count to a host computer; rather, the emulator of the Leary et al. reference is a parallel system, operating upon the same inputs and generating the same outputs as the target device.

Applicants therefore respectfully submit that amended claim 5 and its dependent claims 6, 7, and 18 are novel over the Leary et al. reference.

Applicants also respectfully submit that amended claim 7 is further novel over the Leary et al. reference. The Examiner asserted that the reference teaches the reconfiguring of operating

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[3] Specification, *supra*, at page 19, lines 1 through 11.
[4] Specification, *supra*, page 3, line 25 through page 4, line 21.
[5] Leary et al., *supra*, column 2, lines 45 through 65.
[6] Leary et al., *supra*, column 2, lines 62 and 63; column 4, lines 55 through 61.
[7] *Id.*

parameters for the target DSP.[8] Applicants respectfully submit that there is no defining[9] of operating parameters for the target DSP disclosed in the Leary et al. reference. Rather, the cited locations of the reference do not disclose the defining of operating parameters for the *target* DSP; to the extent that operating parameters are "defined" (or even "reconfigured"), these cited locations of the reference refer only to the emulating system including the digital signal analyzer. And amended claim 7 further requires the configuring of the target DSP operating system responsive to these defined parameters[10]; the Leary et al. reference discloses no such operating system configuration whatsoever, much less for the target DSP (as opposed to the emulating system).

For these additional reasons, Applicants respectfully submit that claim 7 is further novel over the Leary et al. reference.

Applicants further respectfully submit that there is no suggestion from the prior art to modify the teachings of the Leary et al. reference in such a manner as to reach the requirements of amended claim 5 and its dependent claims.

As mentioned above, the Leary et al. reference is directed to an emulation system, in which the very same digital signals presented to the target device are also input to the emulating digital signal analyzer, so that the emulator can determine whether the signal output from the target device are correct.[11] The Leary et al. reference provides no disclosure or suggestion of any reason why one would modify its teachings to have the target DSP chip accumulate (or transfer) any count from which statistics are to be interpreted and processed by the host computer, considering that the emulating digital signal analyzer of the reference is receiving the very same input and output signals as the target. This important difference between the claimed method and the reference results directly from the substantial difference in purpose between the claimed method and the Leary et al. emulator, with the method of claim 7

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[8] Office Action of August 23, 2004, page 3, §2.
[9] As now recited in the claim, instead of "reconfiguring".
[10] *See* specification, *supra*, at page 9, line 9 through page 10, line 2.
[11] *See* Leary et al., *supra*, column 3, lines 53 through 57.

extending further, to the configuring of the target device operating system as a result of the analysis.[12]

For these reasons, Applicants respectfully submit that amended claim 5 and its dependent claims are novel and patentably distinct over the Leary et al. reference.

As mentioned above, claims 8 through 19 and 22 were rejected under §103 as unpatentable over the Leary et al. reference. Claim 8 is amended to overcome the rejection, by clarifying its patentability over the prior art.

Amended claim 8 now specifically requires the step of configuring an operating system of a target DSP responsive to information that is input via a graphical user interface. The method of amended claim 8 now further requires the steps of operating the target DSP to execute an application program, during which the target DSP accumulates at least one count of occurrences of an object; this count is then communicated to the host, which analyzes the operation of the target DSP responsive to the communicated count. The specification clearly supports this amendment to claim 8[13]. No new matter is presented.

Claim 9 is amended to now depend upon amended claim 8, and thus for consistency with that claim; the parameters recited in claims 13 through 15, which depend on claim 9, are consistent with this amendment to the claim. Claim 10 is amended to more specifically recite the steps for operating the target DSP to acquire counter contents from which interrupt latency can be analyzed by the host computer.[14] Claim 11 is amended to more specifically recite the steps for operating the target DSP to acquire counter contents from which CPU load can be analyzed by the host.[15] Claim 12 is amended to more specifically recite the steps for operating the target DSP to acquire counter contents from which interrupt jitter can be analyzed by the host.[16] And claim 22 is amended to more specifically recite the steps for operating the target

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[12] Specification, *supra*, page 3, line 25 through page 4, line 21; *see also* amended claim 7.
[13] Specification, *supra*, at page 10, line 4 through page 12, line 20; page 13, line 21 through page 14, line 21.
[14] *See* specification, *supra*, at page 10, line 4 through page 11, line 11.
[15] *See* specification, *supra*, at page 15, line 9 through page 16, line 9.
[16] *See* specification, *supra*, at page 17, lines 4 through 16.

DSP to acquire counter contents from which maximum CPU busy time can be analyzed by the host.[17] No new matter is presented by these amended dependent claims.

The method of amended claim 8 and its dependent claims provide important advantages over the prior art, including the ability to configure a target DSP operating system, and to monitor and analyze its real-time execution of an application program under that operating system, without requiring undue overhead on the part of the target DSP by offloading the analysis to the host device. The target DSP is only required to maintain certain count values, which does not occupy substantial computational resources on the part of the target DSP, thus enabling the host analysis to reflect real-time operation.

As argued above relative to amended claim 5, Applicants submit that amended claim 8 and its dependent claims are patentably distinct over the Leary et al. reference. Nowhere does the Leary et al. reference anywhere disclose the accumulating of a count of occurrences of an object in a counter at the target DSP, nor does it anywhere disclose the transferring of the contents of this counter to the host for processing and interpreting, both as required by amended claim 8. Instead, the Leary et al. reference teaches an emulation system in which a digital signal analyzer is connected directly to the inputs and outputs of the target DSP device,[18] with all counts and other statistics accumulated and maintained by the emulating system, rather than the target device itself.[19]

There is no suggestion from the Leary et al. reference itself, nor from other prior art of record in this case, to modify the teachings of the Leary et al. reference to accumulate these statistics at the target DSP, much less to then transfer the parameters to a host system. Rather, as mentioned throughout the Leary et al. reference, its emulator operates in parallel "upon the same samples of the analog input and output signals that are being processed by the target system"[20]. This different purpose of the Leary et al. reference, relative to the claimed method, negates any motivation to modify the Leary et al. system to permit the target device to

[17] *See* specification, *supra*, page 15, lines 9 through 22.
[18] Leary et al., *supra*, column 2, lines 45 through 65.
[19] Leary et al., *supra*, column 2, lines 62 and 63; column 4, lines 55 through 61.
[20] *Id.*

accumulate statistics; the very same inputs and outputs are received by the Leary et al. emulator, one simply would not consider employing the target DSP to gather any such data in the Leary et al. system.

For these reasons, Applicants respectfully submit that amended claim 8 and its dependent claims are patentably distinct over the Leary et al. reference.

Applicants further respectfully submit that dependent amended claims 9 through 12 and 22 are further patentably distinct over the Leary et al. reference. While the Examiner asserts that various monitored parameters such as interrupt latency, CPU load, interrupt jitter, wait time, etc. are known in the art (despite not being taught by the Leary et al. reference),[21] Applicants submit that there is no suggestion from the reference to monitor these higher level operating parameters. A fair reading of the Leary et al. reference indicates that its emulation is directed primarily to analyze performance of the target chip as it pertains to the physical electrical signals (*e.g.*, the analysis of "eye" patterns at the inputs and outputs[22]). In contrast, the higher level operating parameters of interrupt latency, interrupt jitter, maximum CPU busy period, CPU load, etc., that are analyzed according to dependent claims 9 through 12 and 22 are qualitatively different as a class from signal voltages and timing as analyzed by the Leary et al. reference. And the specific steps now required in these amended claims, pertaining to the maintaining of counters at the target DSP, are clearly not suggested by the Leary et al. reference. One in fact is left to wonder how the operating of the target device using its counters could possibly assist in the analyzing of the "eye" diagrams with which the Leary et al. reference is concerned.

For these reasons, Applicants respectfully submit that amended dependent claims 9 through 12, and 22, are further patentably distinct over the applied prior art.

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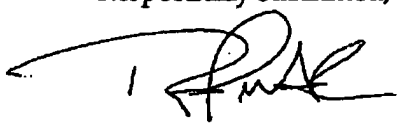
[21] Office Action, *supra*, page 5.

[22] *See* Leary et al., *supra*, column 8, lines 21 through 37; Figure 7.

For the above reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of the above-referenced application is therefore respectfully requested.

Respectfully submitted,



Rodney M. Anderson
Registry No. 31,939
Attorney for Applicants

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9554

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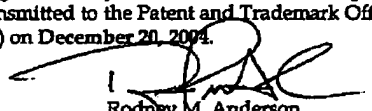

Rodney M. Anderson
Registry No. 31,939